VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus for generating a region of graphics on a display, the apparatus comprising:

a bus having a first address range and a second address range;

a [register] plurality of registers within said first address range configured to store [coordinates] an X coordinate and a Y coordinate of a pixel to be drawn on [the] said display;

a memory within said second address range;

a calculation circuit configured to calculate an address [of a location in a memory] in said second address range for storage of data corresponding to said pixel in dependence on said X and said Y coordinates; and

a control circuit configured to control [said register and said calculation circuit to cause] writing of said data [to be written to and stored] in said memory at said address.

3. (AMENDED) The apparatus as claimed in claim 1, further comprising:

a clipping circuit for (i) comparing said X and said Y coordinates with predetermined clipping limits and (ii) generating a clipping signal configured to indicate [clipping] that at least one of said X and said Y coordinates falls outside said predetermined clipping limits.

4. (AMENDED) The apparatus as claimed in claim 3, wherein said control circuit is further configured to [control] inhibit writing of said data to said address [in said memory,] in response to said clipping signal.

5. (AMENDED) The apparatus as claimed in claim 3, wherein said control circuit is further configured to [control the] prevent calculation of said address [in said memory] in response to said clipping signal.

6. (AMENDED) The apparatus as claimed in claim 3, wherein [said clipping circuit and said calculation circuit are further configured to calculate said address and cause] said data is discarded [to be written to and stored at said address in said memory when said X and Y coordinates fall within said predetermined clipping limits and not calculate said address] when at least one of said X and said Y coordinates fall outside said predetermined clipping limits.

7. (AMENDED) The apparatus as claimed in claim [2] 1, wherein [said] (i) a first register of said registers is memory mapped to a first location and a second location in said [memory] first address range and [said] (ii) a second register of said

registers is memory mapped to a third location and a fourth location in said [memory] first memory range.

8. (AMENDED) The apparatus as claimed in claim 7, wherein said apparatus further comprises:

an address decoder for (i) monitoring said first, said second, said third and said fourth memory locations and (ii) applying a location signal to said control circuit representative of an address location being written to.

9. (AMENDED) The apparatus as claimed in claim 8, wherein said control circuit is further configured to control said first and said second registers and said calculation circuit[,] in response to [a receipt of] said location signal [from said address decoder].

10. (AMENDED) The apparatus as claimed in claim 9, wherein said control circuit is further configured to instruct said calculate circuit to calculate said address [for a pixel coordinate] in response to one of the following:

[a] said X coordinate being [sent to the first register at] written to a preselected one of said first and said second locations; and

[a] said Y coordinate being [sent to the second register at] written to a preselected one of said third and said fourth locations.

11. (AMENDED) [An] The apparatus [for generating a region of graphics on a display, the apparatus] as claimed in claim 1, further comprising:

[a register for storing coordinates of a pixel to be drawn;

a calculation circuit for receiving said coordinates from said register and calculating an address of a location in a memory for storage of data corresponding to said pixel in dependance on said coordinates;

a control circuit for controlling said register and said calculation circuit to cause said data to be written to and stored in said memory at said address;]

a style table for storing data corresponding to a predetermined pattern [or style] for said pixel [to be drawn]; and

a style counter for (i) indexing said data in said style table and (ii) generating a style data signal corresponding to said indexed data.

13. (AMENDED) The apparatus as claimed in claim 11, wherein said style table is [large enough] configured to store [the longest] a non-repeating bit pattern [required] up to a predetermined length for a drawing operation.

14. (AMENDED) The apparatus as claimed in claim [13] 11, wherein [said] (i) a first register of said registers is memory mapped to a first location, a second location, a third location and a [to] fourth location [group] in said [memory] first address range and [said] (ii) a second register of said registers is memory mapped to a fifth location, a sixth location, a seventh location and an [to] eighth location [group] in said [memory] first address range; and

said apparatus further comprising an address decoder for (i) monitoring said first to [further and said fifth to] said eighth [location groups] locations, (ii) generating [applying] a location signal [to said control circuit] representative of an address location being written to and (iii) indexing said style counter in response to [the] said address location being written to.

15. (AMENDED) An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register accessible via a bus for storing coordinates of a pixel to be drawn on said display;

a calculation circuit for [receiving said coordinates from said register and] calculating an address [of a location] in a memory accessible via said bus for storage of data corresponding to said pixel in response to said coordinates; and

a control circuit for controlling said register and said calculation circuit to cause said data to be [written to and] stored in said memory at said address, wherein said calculation circuit is configured to output said address in a first part and a second part, [the] said first part comprising a word address corresponding to [the calculated] said address [location] in said memory and representing a single memory word and [the] said second part comprising a bit address representing a position of [the] said pixel data within [the] said single memory word.

16. (AMENDED) The apparatus as claimed in claim 15, further comprising:

a second register for storing said pixel data in said single memory word prior to said single memory word being written to said [calculated] address [location] in said memory[, said register being capable of storing one memory word]; and

a multiplexer for writing data to said register in dependence on said [word] address [or said bit address] calculated by said calculation circuit.

17. (AMENDED) The apparatus as claimed in claim 16, wherein said multiplexer combines data for at least two [or more] pixels to be drawn in dependence on [the word] said address of each of said pixel to permit storage of [the] said data for said [two or more] pixels in [a] said single memory word.

18. (AMENDED) The apparatus as claimed in claim 17, further comprising:

a comparator connected to said calculation circuit for (i) receiving said [word] addresses, (ii) comparing [the word] said addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if said [word] addresses are identical.

19. (AMENDED) The apparatus as claimed in claim 18, wherein said control circuit is further configured to combine said data for said pixels in response to a receipt of said same address signal [to control said multiplexer to combine said data for said two or more pixels to be drawn].

20. (AMENDED) A method of generating a region of graphics on a display, the method comprising:

(A) storing an [receiving] X [and Y coordinates of] coordinate for a pixel to be drawn in said region in a first address range of a bus;

(B) storing a [storing said X and] Y [coordinates] coordinate for said pixel in said first address range;

(C) calculating an address [of a location in a memory] in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

(D) controlling writing of [causing] said data [to be written to and stored in said] in a memory at said address.

21. (AMENDED) The method as claimed in claim 20, further comprising:

comparing said X and said Y coordinates with predetermined clipping limits; and

discarding said pixel data in response to at least one of said X and said Y coordinates exceeding said predetermined clipping limits.

22. (AMENDED) The method as claimed in claim 20, further comprising:

memory mapping a first register storing said X coordinate to a first location and a second location in said [memory] first address range; and

memory mapping a second register storing said Y coordinate to a third location and a fourth location in said [memory] first address range.

23. (AMENDED) The method as claimed in claim 22, further comprising:

monitoring said first, said second, said third and said fourth locations for a write.

24. (AMENDED) The method as claimed in claim 23, further comprising:

calculating said [memory] address for [a] said pixel [coordinate] in response to one of the following:

[a] said X coordinate being written to [sent to the first register at] a preselected one of said first and said second locations; and

[a] said Y coordinate being written to [sent to the second register at] a preselected one of said third and said fourth locations.

25. (AMENDED) The method as claimed in claim 20, further comprising:

storing style data corresponding to a predetermined pattern [or style] for [each] said pixel;

indexing said style data; and

generating a style data signal corresponding to said [indexed] style data as indexed[; and

causing said data to be written to and stored in said memory at said address].

26. (AMENDED) [A] The method as claimed in claim 25, further comprising:

selecting a color for said pixel to be drawn in dependence on said style data signal.

27. (AMENDED) The method as claimed in claim 20, further comprising:

storing said [pixel] data in a single memory word prior to [a word address] said single memory word being written to said address in said memory[; and

storing said data in said single memory word] in dependence on the word address or a bit address].

28. (AMENDED) The method as claimed in claim 20, further comprising:

combining data for at least two [or more] pixels to be drawn in dependence on a word address of each of said [two or more] pixels to permit storage of [the] said data for said [two or more] pixels in a single memory word.

29. (AMENDED) The method as claimed in claim 28, further comprising:

comparing [the] said word address of consecutive pixels to be drawn; and

combining said data for said [two or more] pixels [to be drawn] if said word addresses are identical.

30. (NEW) an apparatus for generating a region of graphics on a display, the apparatus comprising:

means for storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

means for storing a Y coordinate for said pixel in said first address range;

means for calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

means for controlling writing of said data in a memory at said address.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus for generating a region of graphics on a display. The apparatus generally comprises a bus, a plurality of registers, a memory, a calculation circuit and a control circuit. The bus may have a first address range and a second address range. The registers may be within the first address range and configured to store an X coordinate and a Y coordinate of a pixel to be drawn on the display. The memory may be within the second address range. The calculation circuit may be configured to calculate an address in the second address range for storage of data corresponding to the pixel in dependence on the X and the Y coordinates. The control circuit may be configured to control writing of the data in the memory at the address.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 6 lines 8-10, page 6 lines 16-21, page 7 lines 25-28, page 11 lines 15-18, page 14 lines 2-25 and FIGS. 2 and 4 as originally filed. Thus, no new matter has been added.

INFORMATION DISCLOSURE STATEMENT

The Information Disclosure statement filed December 19, 2000 included references received from an international search report. The relevant portions cited by the searching authority were:

JP2000182024A See abstract, Fig. 3.

JP080187243 A See abstract (WPI, PAJ).

JP080187243 A See ref to 'Address convertor 83'.

JP070296188 A See abstract (PAJ), address generator 12.

JP040349496 A See abstract.

CLAIM OBJECTIONS

The objections of claims 12-14 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3 and 20 under 35 U.S.C. §102(b) as being anticipated by Lee et al. '753 (hereafter Lee) has been obviated by appropriate amendment and should be withdrawn.

Lee discloses a video system with parallel attribute interpolations (Title). Lee does not appear to disclose or suggest every element as arranged in the pending claims. As such, the pending claims are fully patentable over the cited reference and the rejection should be withdrawn.

In particular, pending claim 1 provides (A) a bus having a first address range and a second address range, (B) a plurality of registers within the first address range configured to store an X coordinate and a Y coordinate of a pixel and (C) a memory within the second address range for storing data corresponding to the pixel. In contrast, FIGS. 1B and 10D of Lee appears to disclose a left accumulator 60 on a first bus 82, a right accumulator 62 on a second bus 80 and frame buffers 472 and 474 on a third bus 470. Lee appears to be silent regarding the accumulators and the frame buffers being within a first address range and a second address range on a bus. Therefore, Lee does not appear to disclose or suggest (A) a bus having a first address range and a second address range, (B) a plurality of registers within the first address range configured to store an X coordinate and a Y coordinate of a pixel and (C) a memory within the second address range for storing data corresponding to the pixel as presently claimed. Pending claim 20 and 30 provide similar claim language. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 4 and 5 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Ashburn '106 is respectfully traversed and should be withdrawn.

The rejection of claims 6 and 21 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Foley et al., Computer Graphics: Principles and Practice, 2d Edition (hereafter Foley) is respectfully traversed and should be withdrawn.

The rejection of claims 7 and 22 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Krenik et al. '087 (hereafter Krenik) is respectfully traversed and should be withdrawn.

The rejection of claims 8-10 and 23-24 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Chiu et al. '391 (hereafter Chiu) is respectfully traversed and should be withdrawn.

The rejection of claims 11, 12, 25 and 26 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Prouty '658 is respectfully traversed and should be withdrawn.

The rejection of claim 14 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Prouty, Krenik and Chiu is respectfully traversed and should be withdrawn.

The rejection of claims 15-19 and 27-29 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Ozcelik et al., Patent Publication No. 2002/0149626 (hereafter Ozcelik), is respectfully traversed and should be withdrawn.

Lee teaches a video system with parallel attribute interpolations (Title). Ashburn teaches a method and apparatus for vertex sorting in a computer graphics system (Title). Foley

teaches basic raster graphics algorithms for drawing 2D primitives (Title). Krenik teaches sequential access memories, systems and methods (Title). Chiu teaches a scaleable refresh display controller (Title). Prouty teaches a method and apparatus for raster computer graphic display of rotation invariant line styles (Title). Ozcelik teaches a display unit architecture (Title). The Office Action has not established a *prima facie* case of obviousness for combining Lee with Ashburn, Foley, Krenik, Chiu, Prouty and/or Ozcelik for lack of motivation. As such, the pending claims are fully patentable over the cited references and the rejections should be withdrawn.

In particular, page 4, item 7, lines 8-9 of the Office Action assert that motivation to combine Lee and Ashburn would be to "increase performance levels in graphics systems." Asserting improvements as a motivation is a conclusory statement and not evidence. The Office Action does not explain why one of ordinary skill in the art would seek the particular proposed modifications that would result in the improvements. Instead, the Office Action appears to have used the pending claims as a template to define the proposed modifications that result in the improvements. The improvements then appear to be asserted as motivation for making the modifications. In contrast, the Office Action should have established some motivation or suggest to make the proposed modifications that resulted in the alleged improvements.

Therefore, the motivation asserted in the Office Action does not appear to be clear and particular.

Furthermore, the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination. The factual inquiry whether to combine references must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to combine references is necessary to avoid the subtle but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the combination of references, simply to use that which the inventor taught against its teacher. As such, because the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination, the Office Action does not appear to have met the Office's burden of factually establishing a *prima facie* case of obviousness (MPEP §2142). As such, the pending claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Page 5, item 8, lines 8-9 of the Office Action assert that motivation to combine Lee with Foley is "for both quicker processing and more accurate displays." As argued above for

combining Lee with Ashburn, such conclusory statements are not evidence of motivation. The Office Action has not established some motivation or suggestion to make the proposed modifications that resulted in the alleged improvements. Therefore, the motivation asserted in the Office Action does not appear to be clear and particular. As such, the pending claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Page 6, item 10, lines 8-10 of the Office Action assert that motivation to combine Lee with Krenik and Chiu is that "address decoders are conventionally used to access memory locations and because it allows the locations in the registers to be translated into a memory location." The first assertion that address decoders are conventional does not provide evidence for motivation or suggestion to combine the references (MPEP §2143.01). The second assertion that the combination allows the locations in the registers to be translated into a memory location appears to be paraphrasing the claim language as the motivation. However, the claims may not be used as a template in combining the references. Therefore, the motivation asserted in the Office Action does not appear to be clear and particular. As such, the pending claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Page 5, item 9, lines 9-10 of the Office Action assert that motivation to combine Lee with Krenik is that "this type of memory accessing procedure is conventional as shown by Krenik." Simply because the references could be combined is not sufficient to establish motivation to combine (MPEP §2143.01). The Office Action appears to have failed to provide evidence of why one of ordinary skill in the art would be motivated to combine the references. Therefore, the motivation asserted in the Office Action does not appear to be clear and particular. As such, the pending claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Page 8, item 11,. lines 7-8 of the Office Action assert that motivation to combine Lee with Prouty would be to "provide for drawing complex line styles in real time." Adding a new capability to an invention because then the invention will have the new capability is circular logic that does not establish motivation. The Office Action has not provided clear and particular evidence why one of ordinary skill in the art would be motivated to modify the teaching of Lee to add a complex line style drawing capability as taught by Prouty. As such, the pending claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Page 9, item 12, line 11 of the Office Action asserts that motivation to combine Lee with Prouty, Krenik and Chiu is to

"reduce the time required to access data". Again, simply asserting that an improvement may be achieved is not clear and particular evidence of motivation to make a combination. Furthermore, the fact that four references need to be combined to teach every element of the pending claim 14 generally suggests that the pending claim was improperly used as a template for the proposed combination. Therefore, the motivation asserted in the Office Action does not appear to be clear and particular. As such, the pending claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Page 10, item 13, lines 5-6 of the Office Action assert that motivation to combine Lee with Ozcelik is "to reduce complexity and increase flexibility in defining displays." Here too, a conclusory statement is not evidence of motivation. The Office Action does not explain why one of ordinary skill in the art would be motivated to make the proposed modification other that to assert that the proposed modification would be better. However, Title 35 U.S.C. §101 provides that new and useful improvement are patentable subject matter. Following the logic provided in the Office Action leads to the unreasonable result that it would be obvious to combine all electronic inventions involving memories with Ozcelik to reduce complexity and increase flexibility. Therefore, the Office Action has not provided evidence of motivation to combine the references. As such, the pending claimed

invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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